Single Source Publishing: Bury the Hatchet with DITA-OT

Unlocking the Power of DITA Open Toolkit for Seamless Publishing

Ritu Saxena, Snehal Borole

DITA-OT Day

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Synopsys: Our Realm of Endeavour

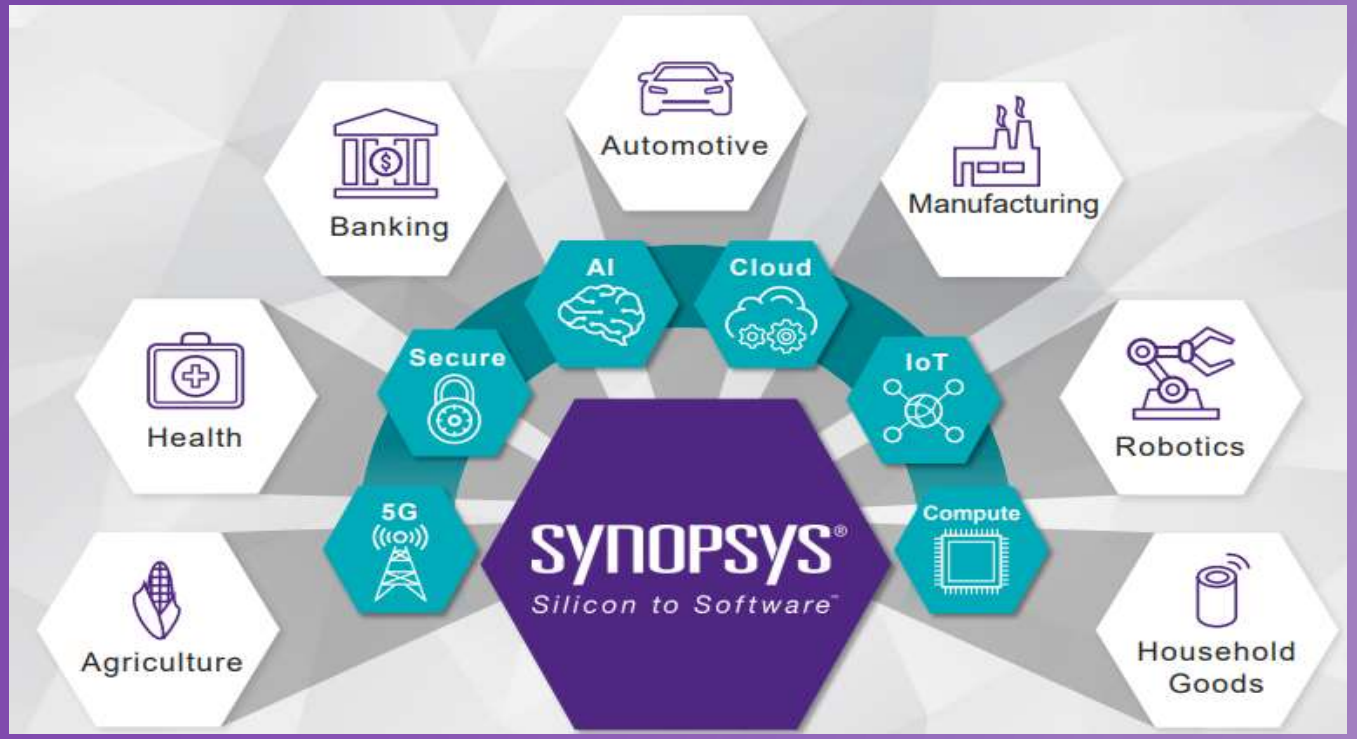
37 Years of Advancing Chip Design

Leading electronic design automation tools and services

Broadest portfolio of foundation, interface, security and processor IP

Pioneer in electronics systems solutions and AI-powered EDA

#12 global software company by revenue



Synopsys drives the trends like: High Speed Networking, Information Security, AI, Cloud Computing, IoT, High Compute Power, and so on.

Synopsys Interface IP Portfolio

Lowest Risk Solutions: Silicon-Proven, Compliant, Secure, Shipping in Volume

High-Performance Compute

PCIe 7.0, 6.0, 5.0, Security

CXL 3.0-1.0, Security

Ethernet 1.6T/800G/400G, Security

HBM 4, 3E/3, 2E/2

LPDDR 6, 5X/5, Security

DDR MRDIMM, 5, 4, 3, 2, Security

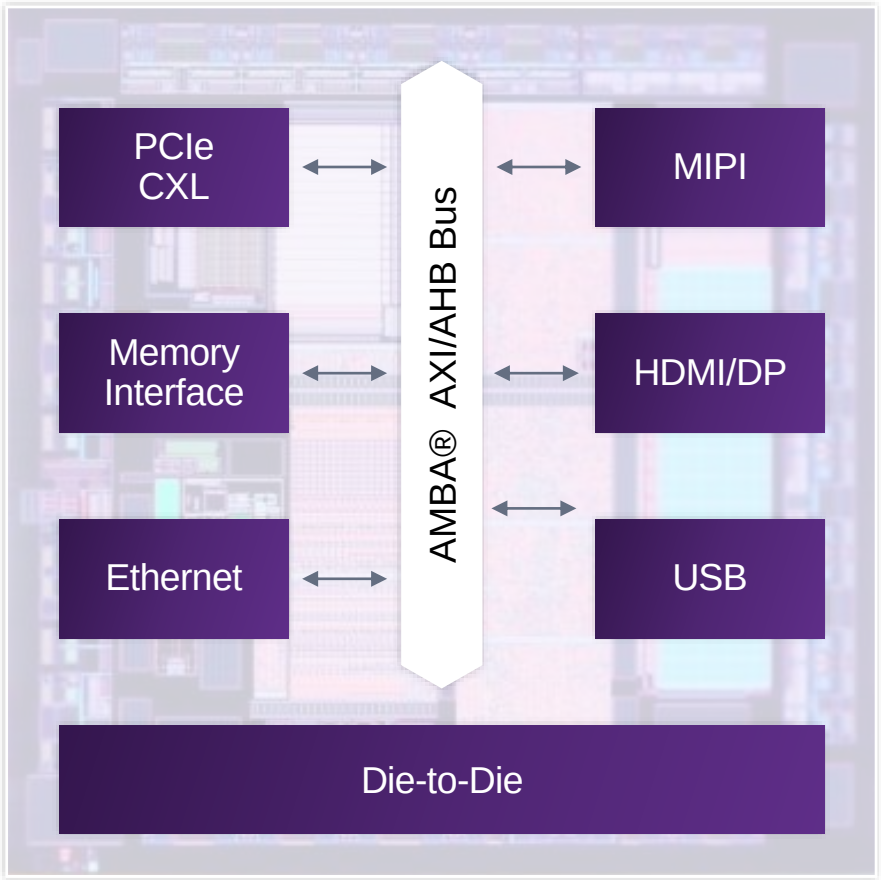
Multi-Die Interfaces

2D UCIe Standard 40/32G

2.5D UCIe Advanced 40/32G

3DIOs

Memory: HBM4, HBM3E/3



Mobile & Consumer

USB 4.0-1.1, Security

PCIe 4.0, 3.0, 2.0, 1.1, Security

MIPI CD-PHY, M-PHY…, Secure UFS

HDMI/DP 2.1 Tx/Rx, Security

LPDDR 6, 5X/5, 4X/4, 3, 2, Security

SD/EMMC

Auto-Grade IP

ASIL B & D Certified, AEC-Q100 Reliability, ISO 9001 Certified Quality Management System

AMBA 2, 3, 4 Interconnect, DMACs, Peripherals, SSI, I2C, I2S, UART

Evolution of IPs

PCI Express: Evolution from 2003 to 2025

Since its launch in 2003, PCI Express has undergone continuous advancements in technology, specification, and transfer speed.

Recent Advancements

PCIe 5.0 caters to **cloud computing** resources with 32G transfer speeds and CXL coherency.

PCIe 6.0 doubled performance to 64G transfer rates using Flow Control Units (FLITS) and PAM4 modulation for **effective, low latency communication and coherency.**

PCIe 7.0 has load-store capabilities and up to 512 GB/s of bandwidth for **secure** data transfers make it possible to connect **multiple accelerators and process large, complex AI and ML models efficiently**

PCIe® Speeds/Feeds - Pick Your Bandwidth

- Flexible to meet needs from handheld/client to server/HPC
- ~Max Total Bandwidth = Max RX bandwidth + Max TX bandwidth
- 35 Permutations yielding 11 unique bandwidth profiles
- Encoding overhead and header efficiency not included

Specifications	Lanes x1	x2	x4	x8	x16
2.5 GT/s (PCIe 1.x +)	500 MB/S	1 GB/S	2 GB/S	4 GB/S	8 GB/S
5.0 GT/s (PCIe 2.x +)	1 GB/S	2 GB/S	4 GB/S	8 GB/S	16 GB/S
8.0 GT/s (PCIe 3.x +)	2 GB/S	4 GB/S	8 GB/S	16 GB/S	32 GB/S
16.0 GT/s (PCIe 4.x +)	4 GB/S	8 GB/S	16 GB/S	32 GB/S	64 GB/S
32.0 GT/s (PCIe 5.x +)	8 GB/S	16 GB/S	32 GB/S	64 GB/S	128 GB/S
64.0 GT/s (PCIe 6.x +)	16 GB/S	32 GB/S	64 GB/S	128 GB/S	256 GB/S
128.0 GT/s (PCIe 7.x +)	32 GB/S	64 GB/S	128 GB/S	256 GB/S	512 GB/S

+ = data rate supported by this and subsequent spec revisions.

DDR: Evolution from 1960 to 2025

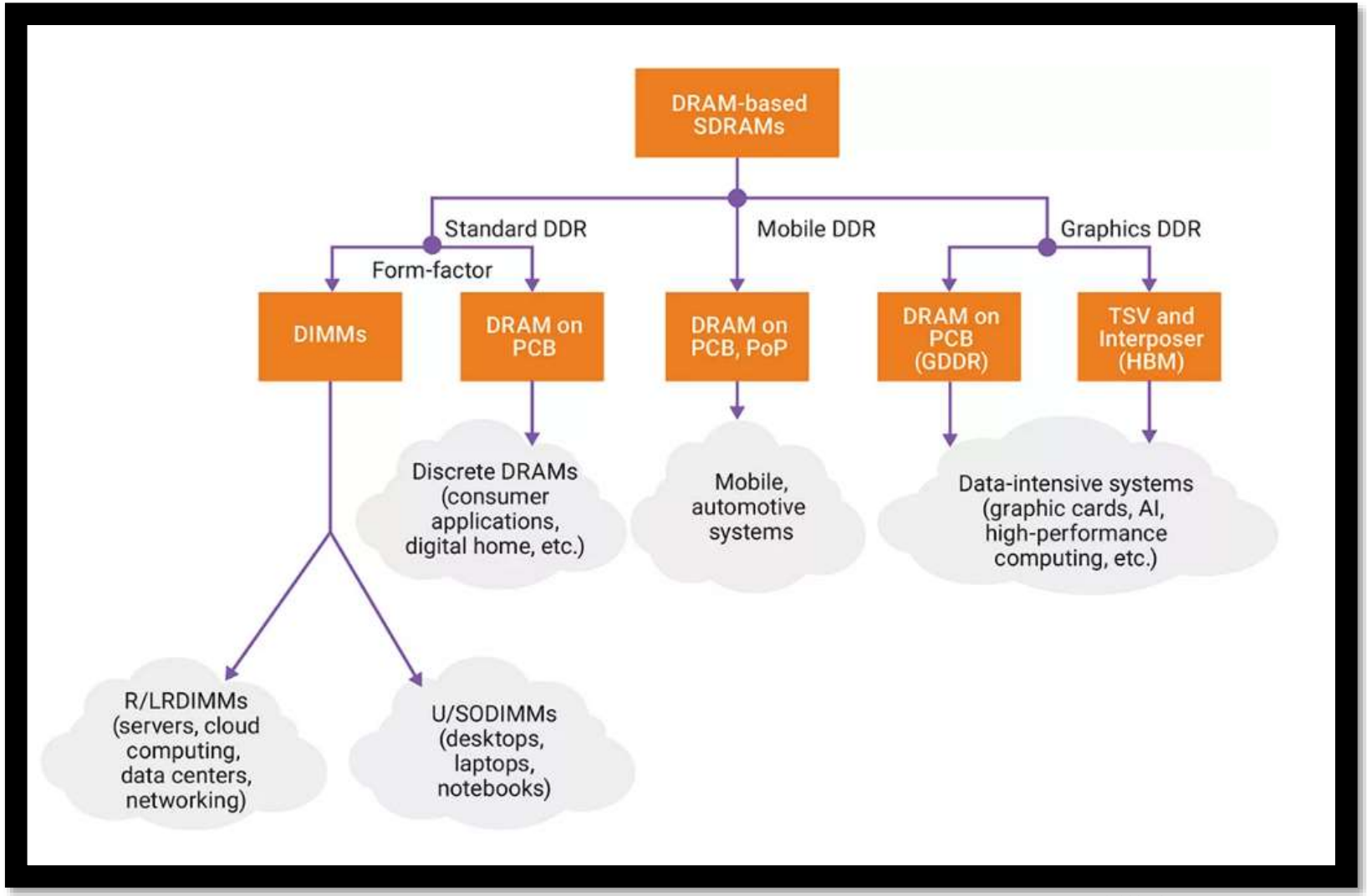
Through 6 generations of advancement, DDR has relentlessly delivered on the need for higher memory capacity, bandwidth, efficiency, and scale.

JEDEC Defined Categories

Standard DDR targets **servers**, **cloud computing**, **networking**, **laptop**, **desktop**, and **consumer applications**, allowing wider channel-widths, higher densities, and different form-factors.

Mobile DDR (LPDDR) targets **mobile** and **automotive applications**, which are very sensitive to area and power.

Graphics DDR (GDDR) targets **data-intensive applications** requiring a very **high throughput**, such as **graphics-related applications**, **data center acceleration**, and **AI**. GDDR and High Bandwidth Memory (HBM) are the standards in this category.



IP Documentation: Simple to Complex

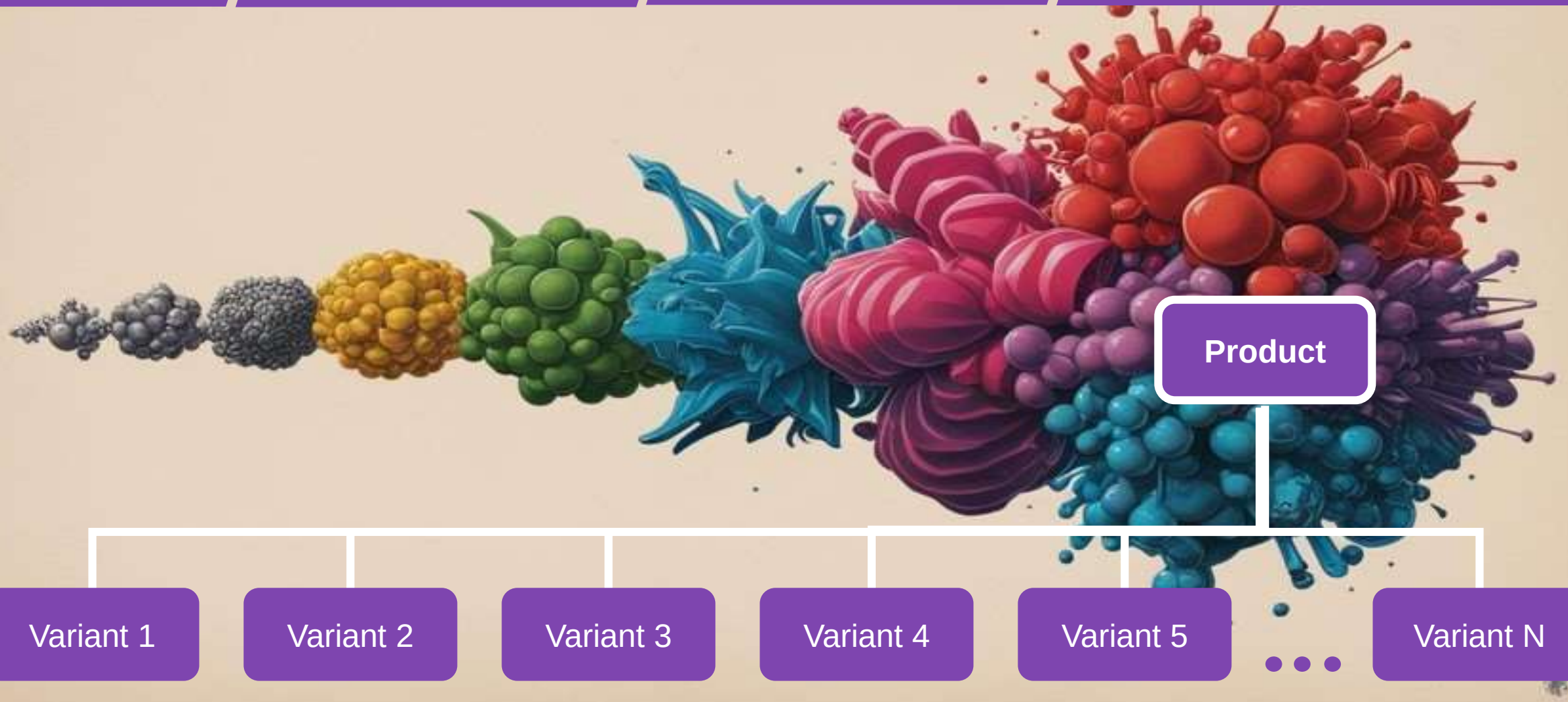
IP Documents Start Simple, Become Complex With Time

PRELIMINARY DOCUMENT
~ 1-2 PDFS
~ 100 PAGES

SUPPORT FOR NEW FEATURES
~ 4-5 PDFS
~ 1000 PAGES

SUPPORT FOR NEW VARIANTS
~ 20 - 30 PDFS
~ 4000 PAGES

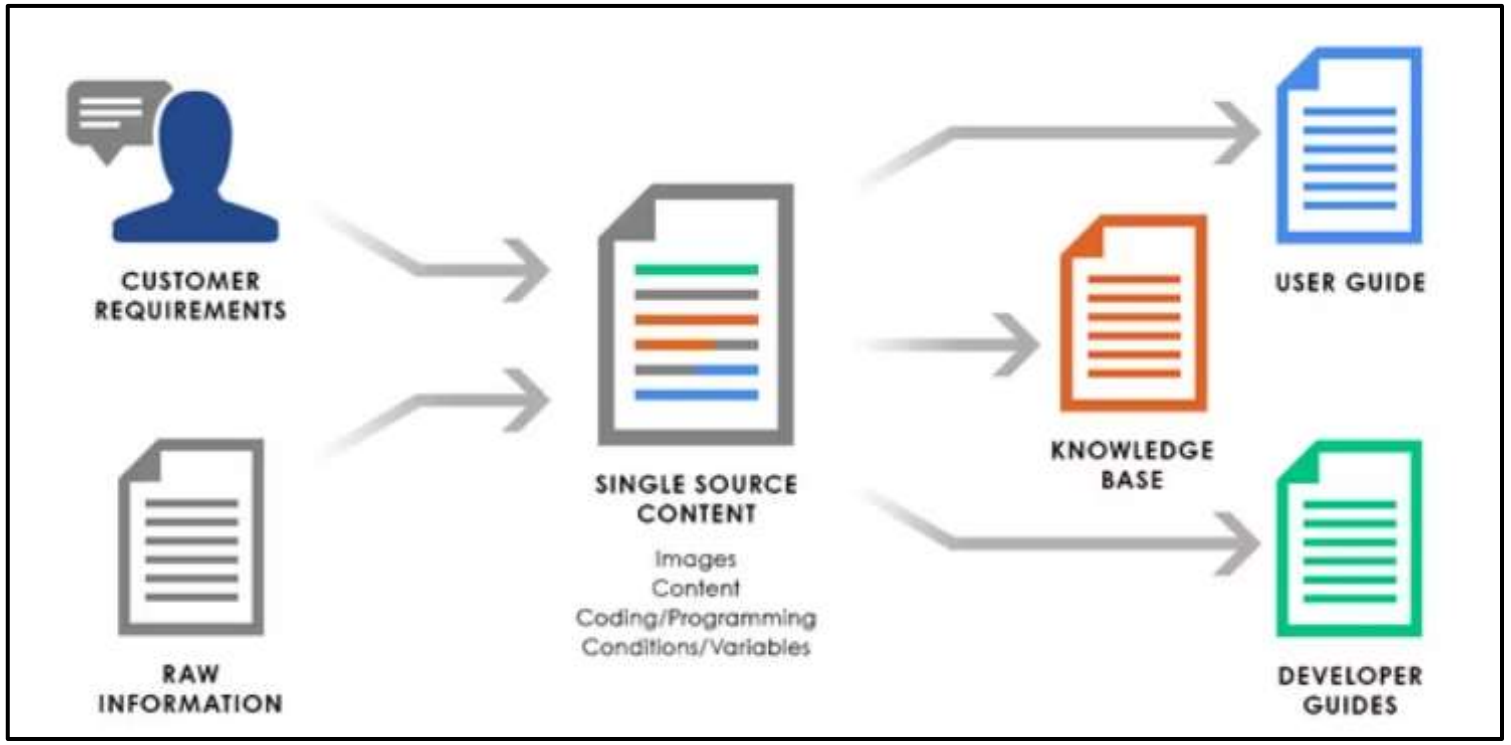
SUPPORT FOR NEW VARIANTS AND FEATURES
~ 20 - 40 PDFS
~ 40000 PAGES



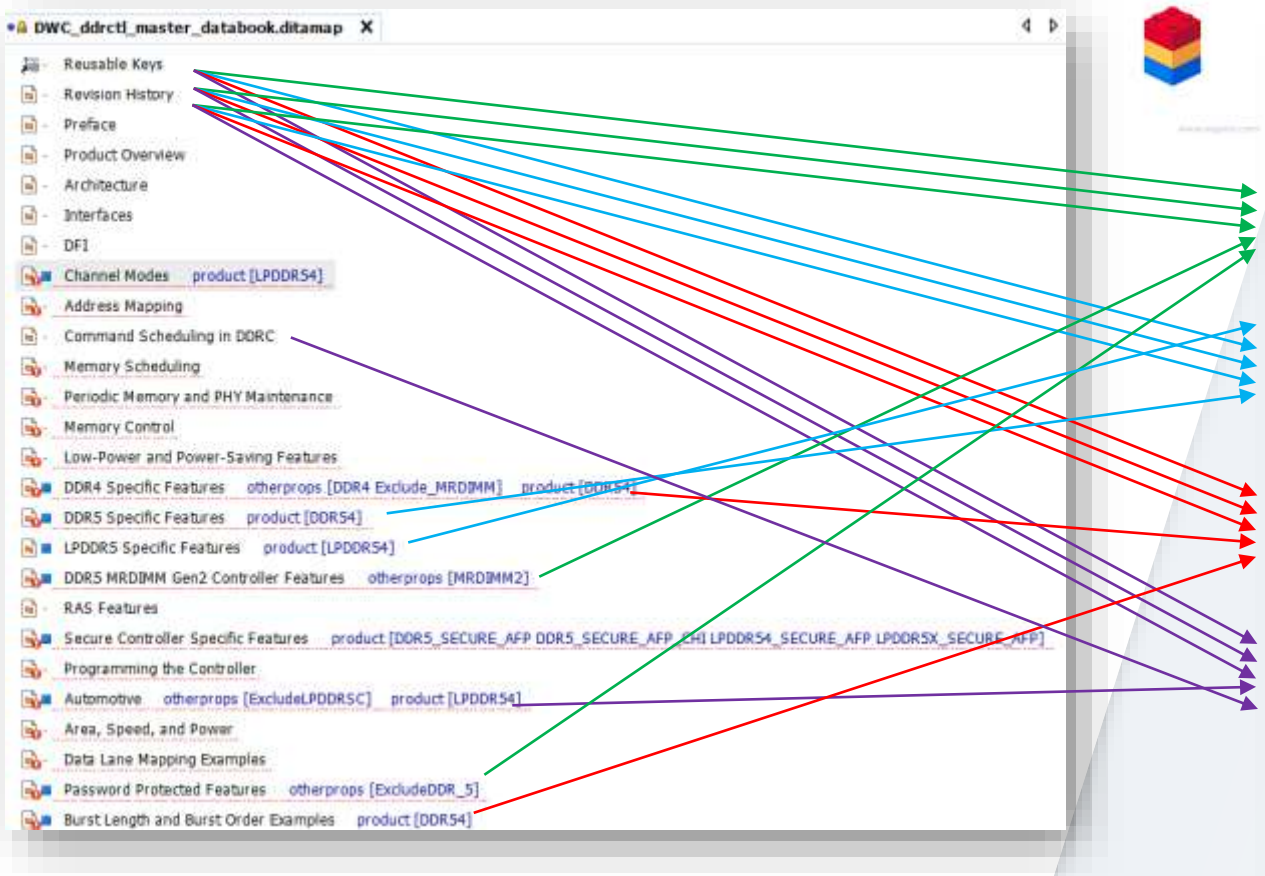
Single Sourcing: The Ideal Solution for Complex Documentation Needs

Why Single Sourcing?

- Content Reuse
- Easier Shared Editing
- Improved Maintenance
- Easier Validation
- Increased Accuracy
- Dynamic Content Management



Single Source Publishing Example



Synopsys DDR IP Solutions

DDR5	+	LPDDR5	+
DDR4	+	LPDDR4	+
DDR3/3L/3U	+	LPDDR3	+
DDR2	+	LPDDR2	+
HBM	+	LPDDR/mDDR	+

Single Sourcing: Challenges

Single Sourcing Challenges

1. What should be the Output file name?

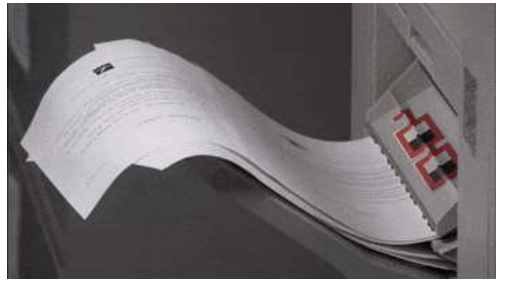
- The tool deduces the output file name from the DITAMAP name.
- How to generate unique output file name for each product variant generated from the DITAMAP?

2. Which DITAVAL file to use?

- DITAVAL files are used to generate different product variants from one DITAMAP.
- How to ensure that the correct DITAVAL file is used to generate a particular product variant?

3. How many files to print?

- Multiple PDFs for a product variant are generated. It is a tedious task to print the entire documentation set repeatedly, at short release intervals.
- How to ensure if the correct documentation set is generated?



DITA-OT Project: Most Elegant Solution for Single Sourced Publishing

DITA-OT Project Files

Context File:
- Contains path to input DITAMAPs
- Contains path to DITAVALs for profiling

Publication File:
- Contains unique transformation parameter details.

Deliverables File:
- Contains reference to context file and publications file.
- For each unique deliverable: Specify input context, output file location, output file name, and publication scenario.

DITA OT Solution for Single Sourcing Challenge 1

Output File Name Setting

Before DITA-OT

- Input File Name:
  DWC_ddr_ctl_databook.ditamap
- Output File Names:
  - For DDR5: **DWC_ddr_ctl_databook.pdf**
  - For DDR4: **DWC_ddr_ctl_databook.pdf**
  - For DDR3: **DWC_ddr_ctl_databook.pdf**

- **No Output Differentiation**
- **Too much Manual Intervention**
- **Error prone**

After DITA-OT

- Input File Name:
  DWC_ddr_ctl_databook.ditamap
- Output File Names:
  - For DDR5: **DWC_ddr_ctl_ddr5_databook.pdf**
  - For DDR4: **DWC_ddr_ctl_ddr4_databook.pdf**
  - For DDR3: **DWC_ddr_ctl_ddr3_databook.pdf**

- **Clear Output Differentiation**
- **No Manual Intervention**
- **Not Error Prone**

DITA OT Solution Single Sourcing Challenge - 2

DITAVAL Selection

Before DITA-OT

- Input: **DWC_ddr_ctl_databook.ditamap**
- **Select DITAVAL during output generation**:
  - For DDR5: ddr5.ditaval
  - For DDR4: ddr4.ditaval
  - For DDR3: ddr3.ditaval

- **Too much Manual Intervention**
- **Error Prone in Concurrent Source file usage scenario**
- **No Validation**

After DITA-OT

- Input File Name: **DWC_ddr_ctl_databook.ditamap**
- **Preset DITAVAL for each output variant in context.xml file**:
  - For DDR5: ddr5.ditaval
  - For DDR4: ddr4.ditaval
  - For DDR3: ddr3.ditaval

- **No Manual Intervention**
- **Error Prone in Concurrent Source file usage scenario**
- **Efficient Validation Scenarios for various Contexts**

DITA OT Solution Single Sourcing Challenge - 3

Generation of Multiple Outputs

Before DITA-OT

- Input: **DWC_ddr_ctl_databook.ditamap**
- Output:
  - For DDR5: **DWC_ddr_ctl_databook.pdf**

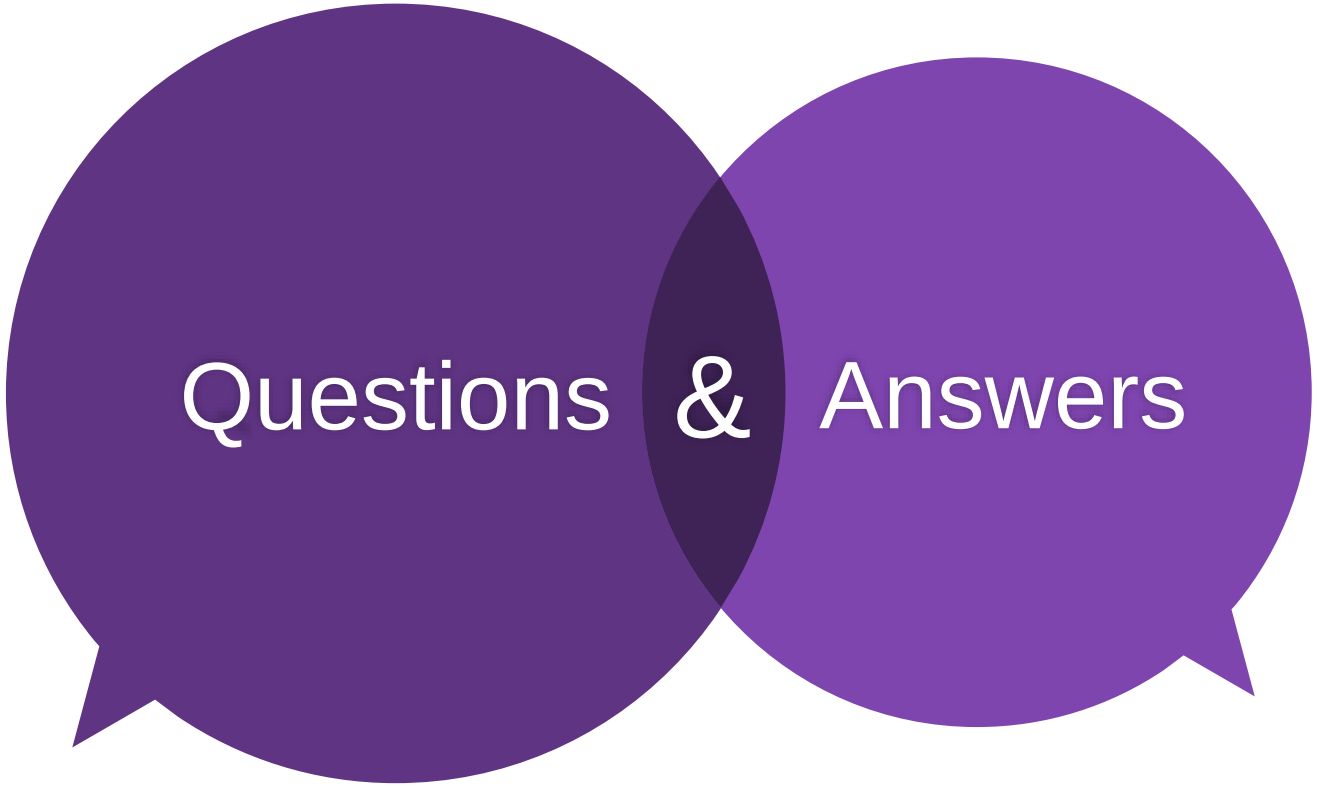
- **One Output per in One Format in one iteration**
- **Time Consuming**

After DITA-OT

- Input: **DWC_ddr_ctl_databook.ditamap**
- Outputs:
  - For DDR5: **DWC_ddr_ctl_ddr5_databook.pdf**
  - For DDR4: **DWC_ddr_ctl_ddr4_databook.pdf**
  - For DDR3: **DWC_ddr_ctl_ddr3_databook.pdf**

- **Generate Single/Multiple Outputs in Single/Multiple Formats**
- **Time Saving**

Live Demo



THANK YOU